REMARKS

In response to the Office Action dated January 30, 2002, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1 and objections to all claims. The indication that claims 2-5 contain allowable subject matter is noted with appreciation.

In response to the objection to the specification, the abstract has been revised to place it in the form of a single paragraph, as well as remove the reference characters and legal terminology.

Claims 1-5 were objected to, on the grounds that they were considered to contain various informalities. In response thereto, each of these claims have been amended as suggested by the Examiner.

Claim 1 was rejected under 35 U.S.C. §102, on the grounds that it was considered to be anticipated by the *Kim et al.* patent (U.S. Patent No. 5,729,004). It is respectfully submitted, however, that the *Kim et al.* patent does not anticipate, nor otherwise suggest, the subject matter of claim 1.

Claim 1 recites a card having a microprocessor and contact via which the card communicates with a terminal. The claim further recites a communication device in the form of a hard-wired circuit disposed between the contacts and the microprocessor. This communication device operates according to an asynchronous communication protocol, to check the integrity of signals transmitted between the microprocessor and a terminal. The claim recites that the communication device "includes means to return at least one item of information to the terminal as a function of the signals received."

The *Kim et al.* patent discloses a data communication device for use in a smart card. In relevant part, this data communication device checks parity calculated from data received from a terminal with the value of a parity bit received from the terminal, to determine whether there was an error in the data received from the terminal. Unlike the invention recited in claim 1, however, there is no disclosure in the *Kim et al.* patent that this data communication device returns at least one item of information to the terminal as a function of signals received.

In connection with this claimed feature of the invention, the rejection of claim 1 refers to the *Kim et al.* patent at column 9, lines 61+. This portion of the patent describes the operation performed by a parity detector 35 in connection with data received from a terminal. Referring to Figure 3, an exclusive NOR gate 37 compares a received parity bit RPB, transmitted by the terminal, with an operation parity bit DPB that is computed in a parity operator 34 on the basis of data received from the terminal. If these two bits match, a NOR gate 38 of the parity detector 35 outputs a parity detection signal PBT at a logic low level, indicating that the data was properly received. On the other hand, if the received parity bit RPB and the operation parity bit DPB do not match, the NOR gate 38 outputs a high level signal, to indicate that the received data is in error.

The patent does not disclose that the parity detection signal PBT is returned to the terminal. Rather, as stated at column 10, lines 19-22, "the *controller of the smart card device* analyzes the logic of the parity detection signal PBT..." Thus, the data communication device of the *Kim et al.* patent provides an item of information that has been computed as a function of the received signals, namely the parity detection signal

PBT, to the microprocessor of the card itself. The patent does not describe what happens if an error condition occurs. It may be the case that the microprocessor attempts to correct the data error. Alternatively, the microprocessor may send a signal to the terminal, requesting retransmission of the data that was erroneously received. There is no disclosure in the *Kim et al.* patent, however, that the data communication device, as opposed to the microprocessor, returns a signal to the terminal as a function of the received data.

Accordingly, it is respectfully submitted that the *Kim et al.* patent does not anticipate Claim 1. Reconsideration and withdrawal of the rejection, and allowance of all pending claims is respectfully requested.

Respectfully submitted,

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Date: April 30, 2002

Attachment to Amendment dated April 30, 2002

Marked-up Copy of the Abstract

The invention relates to cards with a microprocessor [(10)] and contacts [(22)].

The invention lies in the fact that a communication device [(40)] of the asynchronous type is disposed between the contacts [(22)] and the microprocessor [(10)] so as to relieve the microprocessor of the communication tasks and thus allow better use of the central unit [(12)] of the microprocessor [(10)] and the associated memories [(14, 16, 18)]. This device [(40) comprises essentially] includes an analysis circuit [(34)], a circuit [(36)] for checking the integrity of the series of pulses, a circuit [(38)] for determining the characters in the series of pulses and pluralities of registers [(42, 44 and 46)] which are connected with the microprocessor [(10)].

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Marked-up Copy Claims 1-5

1. (Twice Amended) A card with a microprocessor and contacts, and a communication device in the form of a hard-wired circuit disposed between the contacts and the microprocessor and operating according to an asynchronous communication protocol with checking of [the] integrity of signals transmitted between the microprocessor and a terminal, wherein said communication device includes means to return at least one item of information to the terminal as a function of the signals received.

2. (Twice Amended) A card with a microprocessor and contacts according to Claim 1, wherein the communication device comprises:

- a circuit for analysing [the] electrical signals transmitted by [a] the terminal so as to supply a series of electrical pulses,

- a circuit for checking the series of electrical pulses in order to determine the integrity of the series of electrical pulses and to supply a code indicating the status of the check,

- a circuit for determining each character from the pulses in the series,

- a first plurality of registers for recording [the] characters of a command and an address supplied by the character determination circuit and making them available to the microprocessor,

- a second plurality of registers for recording [the] characters of data supplied by the character determination circuit and making them available to the microprocessor,

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Marked-up Copy Claims 1-5

- a circuit for acknowledging the command, associated with the first plurality of registers, for analysing the characters of the command and supplying a code indicating a command reception status,

- a third plurality of registers for recording codes for the data and for the status of execution of the command supplied by the microprocessor, and

- a circuit for transmitting to the terminal the codes supplied by the checking circuit, the command acknowledgment circuit and the third plurality of registers.

3. (Twice Amended) A card with microprocessor and contacts according to Claim 2, wherein the analysis circuit detects the signals transmitted and presents them in the form of a series of binary electrical pulses [of the binary type].

4. (Twice Amended) A card with a microprocessor and contacts according to Claim 2 wherein the checking circuit checks for [the presence of] a binary parity digit or a cyclic redundancy code and supplies a corresponding signal or code.

5. (Amended) A card with a microprocessor and contacts card according to Claim 3, wherein the checking circuit checks for [the presence of] a binary parity digit or a cyclic redundancy code and supplies a corresponding signal or code.